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A Low Power CMOS LC VCO Using 70 nm Technology for C band Applications

Dheeraj Nagar[1], Rajendra Yadav[2]
Department of Electronics and Communication, RGPV Bhopal, SDBCT Indore (M.P.), India[1]
Department of Electronics and Communication, RGPV Bhopal, SDBCT Indore (M.P.), India[2]
dheeraj.nagar1@gmail.com[1] , yadav.raj1985@gmail.com[2]

Abstract: *In this paper, a Low power CMOS LC Voltage Controlled oscillator for C band has been designed. The cross coupled differential LC VCO topology is used to optimize the trade- off between the phase noise and power consumption. A 70nm CMOS technology has been used for wireless applications. To achieve high frequency tuning range a variable MOS capacitance has been used by varying gate voltage of MOS in order to meet this VCO topology for C band applications. Simulation is performed by Tanner EDA 14.0 on 70nm CMOS technology. The tuning frequency of the LC VCO circuit is from 4.99 to 5.38GHz this can obtain by applying the tuning voltage ranging from 1.5 to 2.7 V. This topology dissipates power of 1.40mW at the Maximum oscillation frequency which is very low as compare to conventional VCO.*

Keywords: *Voltage Controlled oscillator (VCO), tuning frequency, tuning range, power consumption, CMOS*

1. INTRODUCTION

Oscillators are important part of many electronic systems which is used from clock generation in microprocessor to carrier synthesis in cellular mobile communication requiring different oscillator topologies and performance parameter. Recently the rapid growth in the field of wireless communication and the advancement in complementary metal oxide semiconductor (CMOS) technology have made it possible to implement high frequency oscillator using CMOS technology. In wireless communication oscillators are required to be tunable over a wide frequency range. The wide frequency range is usually obtained by varying the voltage and the name comes Voltage Controlled Oscillator (VCO). VCO is the unique component in frequency synthesizer for Radio Frequency (RF) for wireless Communication application. Voltage Controlled Oscillators (VCOs) works as a critical component in many wireless RF transceivers and are mostly associated with signal processing tasks like frequency selection and carrier generation. Now a day, RF transceivers required to be programmable carrier frequencies, and commonly rely on phase locked loops (PLLs) to accomplish the same. These PLLs has a less accurate RF oscillator in a feedback loop whose frequency can be controlled by changing control signal. [1-2]

The key performance of a VCO is depending on phase noise at certain range of frequency, tuning range of the frequency, power consumption. The VCO selection is depends on this key performance. The ring VCO and LC VCO topologies provide all the key performance. For wireless application VCO required low phase noise and low power consumption performance. In LC VCO, the phase difference between tank current and tank voltage is zero i.e. LC VCO has inherent filtering capabilities which substantially reduces phase noise to great extend. Due to this unique reason LC VCO is preferred over the ring VCO for wireless applications. [3]

There are many different topologies for designing, LC VCO which have been cited in [4-6]. They are single transistor Oscillator Topology, Cross-coupled differential topology, CMOS core cross-coupled differential topology, Quadrature VCO with reconfigurable LC VCO. One transistor topology has acquired larger transistor area compared to cross coupled differential topology. For this reason cross coupled differential topology is considered more accurate topology than one transistor topology, for fully integrated CMOS VCO. CMOS Core cross coupled topology having higher parasitic capacitance over cross coupled differential topology. Higher the parasitic capacitance means lower the tuning range. Due to this reason CMOS cross coupled topology is not prefer for high frequency range for wireless applications [7-13]. In [14] a switched capacitor array, substrate noise filter and two power supply are involved in the CMOS differential cross coupled topology. This proposed wide band LC VCO used for low phase noise and low power consumption wireless applications.

This paper proposes a cross coupled differential topology for high frequency application and low power consumption. The objective of proposed design is to achieve high frequency operation and low power consumption using 70nm CMOS technology without involving two power supply and switched capacitor array.

Rest of the paper is organized as follows: in section II; basic feedback amplifier model for oscillator & Barkhausen criteria for oscillation is discussed. The proposed cross coupled differential topology & simulation result are discussed in section III. Simulation results are compared in section IV, whereas section V concludes the paper.

2. FEEDBACK MODEL OF OSCILLATOR

A oscillator is a device which produces a periodic output usually in the form of voltage. Oscillators are nonlinear in nature, though are usually viewed as a linear time invariant feedback system as shown in Figure 1. In the s-domain, the transfer function of this negative feedback amplifier system is given by

$$\frac{V_{out}}{V_{in}}(s) = \frac{A(s)}{1 + A(s)F(s)}$$

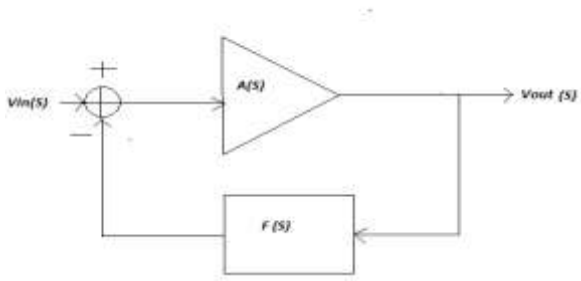

Fig.1. Negative feedback system with frequency selective network.

This system provides a periodic output at frequency S=jω0.If the loop gain A(s) F(s) is equal to -1 at a specific frequency ω0, the closed loop gain approach to infinity. Under this condition the circuit amplifies its own noise component indefinitely and system trends to be unstable. In summary, if a negative feedback circuit has a loop gain that satisfies two conditions:

$$|A(j\omega_0)F(j\omega_0)| \geq 1$$

$$\angle |A(j\omega_0)F(j\omega_0)| = 180$$

The Barkhausen Criteria for oscillation is Compulsory but not sufficient [1].

3. CROSS COUPLED TRANSISTOR TOPOLOGY

The topology which we used in this circuit has parallel combination of LC tank lossy section, cross coupled NMOS transistor pair, current mirror and variable capacitor as shown in figure number 2. LC tank section has capacitor (C), inductor (L) and tank resistance in parallel LC (Rp). Cross coupled MOS transistor pair which provides an equivalent negative resistance .This resistance is used to compensate LC tank equivalent parallel resistance. Due to low noise characteristics of a PMOS device a PMOS cross-coupled transistor pair has been adopted in a VCO design. The PMOS having very small hot carrier effect . This is a very critical case in a CMOS process where hot electron noise is significant. Flicker noise of a PMOS devices is approximate ~10 times smaller than that of a NMOS devices for the equal transistor dimension. Considering that a PMOS transistor has a lower mobility, the flicker noise of a PMOS device should be lower at given current and gm as larger gate area. Due to

this reasons, it has been declared that a VCO using a cross-coupled PMOS pair shows low phase noise characteristics. PMOS devices have to be double the size of NMOS devices to achieve similar trans-conductance parameters. For this reason NMOS cross coupled pair transistor device is more preferred over PMOS cross coupled pair transistor device in this topology [16-18].

In order to get a desirable control over the negative resistance and evidently, the oscillation amplitude, a current mirror is generally taken to limit the supply current. The bias current that flows through current mirror is called as the tail current and it sets the total power dissipation. However, in some cases, it has been observe that it may be advantageous to eliminate the tail current source to get better phase noise characteristics [6].

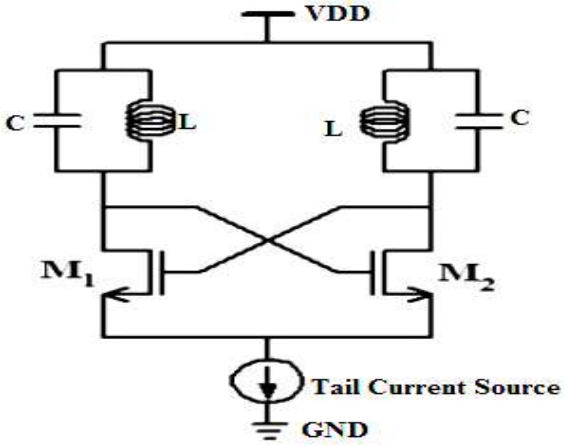

Fig.2. Cross coupled differential topology

4. VCO DESIGN

4.1 MOS Varactor

The MOS capacitor has a structure that is analogous to a parallel plate capacitor with the source, drain and bulk (D, S, and B). In this proposed topology a PMOS transistor connected together realizing one plate of the capacitor and the polysilicon gate constituting the other. The The resulting MOS capacitor is illustrated in Figure 3.

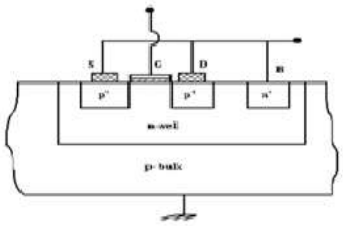

Fig.3. MOS Capacitor.

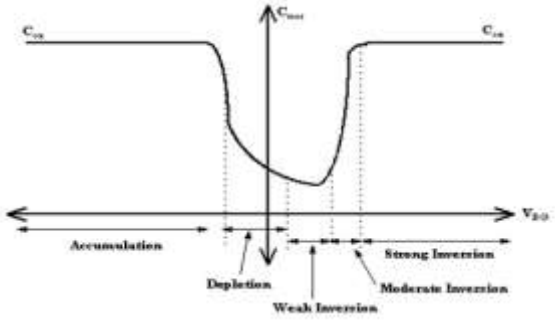

Fig.4. Capacitance versus voltage characteristics

4.2 Final Proposed VCO Design

The schematic circuit diagram of the proposed LC VCO is shown in Fig. 5. The topology of proposed circuit is based on NMOS cross coupled differential LC structure (N-pair) with NMOS is used as a tail current source. The circuit structure once optimized, it performs better than other common VCO topologies, in terms of the power consumption and high frequency of operation for RF application. The better your paper looks, the better the Journal looks. Thanks for your cooperation and contribution.

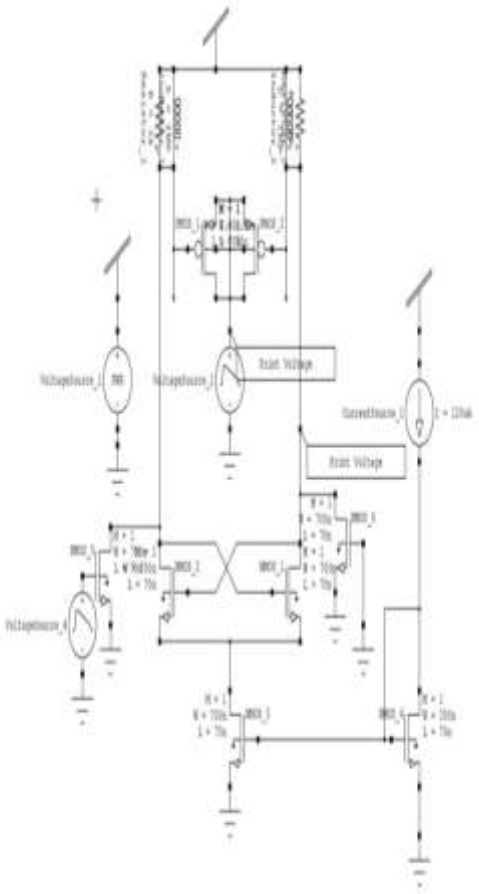

Fig.5. Proposed crossed coupled differential LC VCO topology.

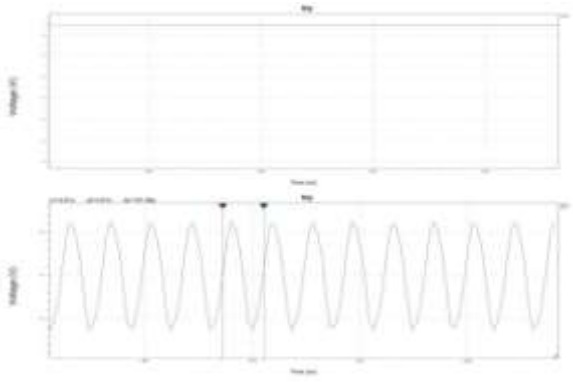

Fig.6. Simulation result of Proposed crossed coupled differential LC VCO topology

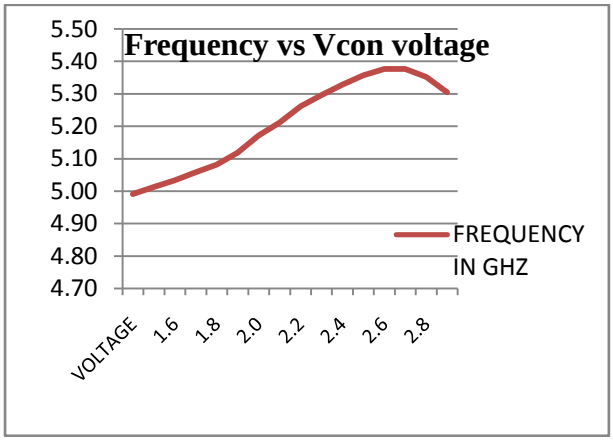

Fig.7. Frequency vs. v_{con} voltage plot.

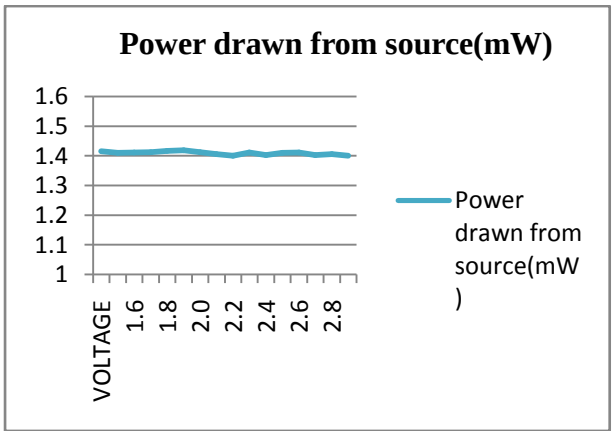

Fig.8. Power drawn from the Source

5. COMPARISON AND DISCUSSION

A comparison of this work with previous wide-tuning range design is shown in Table given below. From this comparison table, it is seen that cross coupled differential LC VCO topology has low power consumption and high frequency for C band applications.

TABLE I.
COMPARISON OF PARAMETER

Mode	This Work	Ref.14
Technology	70nm	65nm
Frequency(in GHz)	4.99-5.38	0.75-1.5
Power Consume	1.4 mW	3.4mW
Tuning Range	1.5-2.7	83%
Tuning Voltage	7.18	--

6. CONCLUSIONS

A low power high frequency cross coupled differential LC VCO topology is realized in the Tanner 14.0 on 70nm CMOS technology for C Band applications. The tuning Frequency range of the VCO is from 4.99 to 5.38 GHz with tuning voltage from 1.5 to 2.7 V while consuming 1.4mW power. The main advantage of this topology is lower-power consumption and also high frequency operation for wireless applications.

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