International Journal of Technology Research and Management
ISSN (Online): 2348-9006
Vol 4 Issue 5 May 2017

A Review on Design and Implementation for Voltage Drop in CMOS

Kamlesh Deware[1], Prof. Madhvi Bhanwar[2]
Dept of Microelectronics & VLSI, Sagar Institute of Research & Technology Truba, Indore[1, 2]
dewarekamlesh@gmail.com[1], madhvi_osr@yahoo.co.in[2]

Abstract: *This paper presents the study and survey analysis on different width size of transistor in CMOS rectifier for output voltage drop. The paper gives information about miniaturizing the CMOS rectifier using two PMOS and NMOS configuration. This investigation focuses on the effect of the width-to-length ratio by using 0.35µm technology. Therefore, increase the width size and minimize the internal resistance. The model is operated at a frequency of 50Hz with an AC voltage source. CADENCE software is used for simulation and designing work.*

Keywords: *CMOS rectifier, AC to DC converter, MOSFET width size, internal resistance of transistor, low frequency.*

1. INTRODUCTION

In recent years, the usage of portable devices such as laptops, Smartphone, computers have been increased to great extent. The recognition and need of these portable electronic devices compels designers to aim for small silicon area, advanced speed, low internal resistance, reduce voltage drop and reliability. But these parameters are major concern in schematic design before their actual implementation in the layout. There are various possible logic styles compared to the basic CMOS logic style.

CMOS rectifier is one of the miniaturized technologies that have been proposed to replace the conventional rectifier. The conventional rectifier has a drawback of high voltage drop in the converter since it has high internal resistance. Then researchers searched a method to replace the converter using Scotty-diode and CMOS technology which have lower voltage drop in the converter different form to the previous design. Nevertheless, Schottky-diode did not consistent with the CMOS technologies; therefore did not suit CMOS design process. So, all the researchers work for low input voltage application on the CMOS rectifier. The use of CMOS rectifier as a converter is in communication area, medical, electronic components and radio frequency identification. Rectifier is an electrical device that converts AC voltage to DC voltage, which flows in only one direction. The process is known as rectification. DC voltage is obtain because if an AC voltage source is applied at the ends of the PN junction diode than we observe that when the junction is in forward bias the current passes through it but when the junction is in reverse bias than no current passes through it.

CMOS RECTIFIER TOPOLOGY:

The conventional rectifiers are constructing by using diodes. Generally, the diodes have large voltage drop and not required for low voltage circuits. The forward voltage for diode is higher. Power loss is greater than the higher forward voltage which is present the problem when using this conventional rectifier. CMOS rectifier solved the problem and reduces the forward voltage drop. Figure 3 shows the CMOS rectifier using two PMOS and two NMOS transistors. Where M1 and M3 are PMOS transistors and M2 and M4 are NMOS transistors. For each cycle, one PMOS and NMOS will turn ON. The CMOS rectifier is designed to have the lower internal resistance and reduce the voltage drop by considering the capability of electron mobility in PMOS and NMOS. Although these CMOS rectifier structure are simple, By using 0.35 µm CMOS technology. This rectifier used to convert input sinusoidal wave from negative half waves into positive, which is possible with two PMOS and two NMOS transistors shown in figure. Hence, the voltage drop can be minimized by using large size of transistors to decrease the resistance and get a small voltage drop. The circuit was simulated with

CADENCE simulation software. A pure sinusoidal waveform whose frequency is 50Hz is applied on the input and load of 2KΩ are used in the rectifier. The voltage efficiency is defined as the fraction of the DC output voltage Vout and the AC input voltage amplitude |Vin|. The efficiency of output voltage is higher with larger load resistors in CMOS rectifier. Generally the circuit cannot work when the input voltage is larger. So, in this paper we design CMOS rectifier to overcome these drawbacks. This rectifier work at a 0.25V at input voltage. The rectifier can achieve a maximum power efficiency of 98%.

The main goals of this paper are the reduction of the voltage drop over the CMOS rectifier and achievement of a high efficiency. In order to reduce voltage drop and power loss from CMOS rectifier to the load resistor. It follows the change of the size of the MOS transistor, as the size increase, the channel resistance will become small. The voltage drop on the channel resistor will less, hence this will increase the output voltage VOUT.

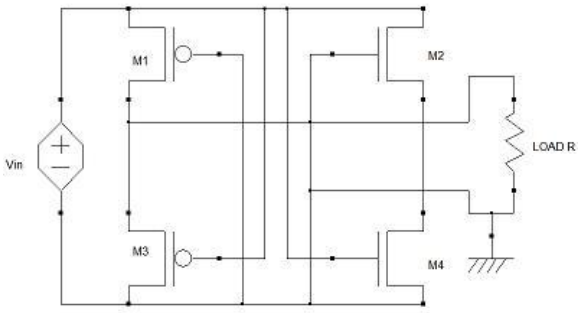

Figure.1 CMOS rectifier circuit

Different Parameters:

For every positive cycle and negative cycle of the input AC voltage in PMOS and NMOS transistors have the internal resistance. In CMOS rectifier, when the width size of PMOS and NMOS transistors are similar or lower than the total resistance is higher and we increase the width size of the PMOS transistor then the total resistance is reduced. It proves that the width size is one of the factors that effect on the internal resistance and voltage drop. The transistor larger width size make the bigger current to go through to the transistor, hence it have the small value of the resistance. The width over length ratio for transistor is 750/1. The CMOS rectifier has lower internal resistance by considering the capability of electron mobility in PMOS and NMOS transistors.

Analysis of width size of transistor on internal resistance in CMOS rectifier

In this analysis, All transistor width size are set to be similar. The designs are varied from small, medium and large width sizes. Thus, the width size of PMOS transistor is varied to improve the drive current and reduce the internal resistance and voltage drop in the circuit. The width size of PMOS transistor is enlarged from 750µm to 1500µm while the width size of NMOS transistor is set at 750µm.These analysis are done to get the lower internal resistance and reduce the voltage drop in CMOS rectifier.

Analysis on the width size of the transistor to the output voltage in CMOS rectifier

The focused on this design is to determine the output voltage using large width size of transistor is 40.6% higher than small width size of transistor. It means that the bigger width gives better output voltage compared to lower width.

Analysis for output power by using different width size of transistor in CMOS rectifier

For the first design configuration, the width size of PMOS and NMOS is set to be similar. The width size of PMOS is varied from 800µm to 1500µm but NMOS width size is set at 750µm. It shows that the variation of output power when the drive current is improved. The output power is constant for designs 1000µm to 1500µm.

Analysisof Power Conversion Efficiency dependence on transistor sizing

This analysis shows PCE dependence on the width size of transistor. The wider version exhibits a slightly larger peak PCE, where width size of PMOS and NMOS transistor is varied from lower to higher. PCE of the rectifier is defined by output power POUT divided by the input power PIN. The sum of the output power and the loss of the rectifier is define the total

input power. PCE can be written as:

$$PCE = P_{OUT} / P_{IN}$$

$$PCE = P_{OUT} / (P_{OUT} + P_{LOSS})$$

2. LITERATURE REVIEW:

A. Description of papers

(1) In 2013, IEEE Mohr Arial Rap, Roskhatijah Radzuan & Mustafar Kamal Hamzah presented the primary works on the

width size of the transistor are varied to investigate the effect on internal resistance in CMOS rectifier using two PMOS and NMOS. The smaller width size resulted in the high internal resistance of CMOS rectifier. The proposed circuit are designed to have the lower internal resistance due to increase the width size, In this work, PMOS transistor width size is designed to be larger than NMOS transistor. The NMOS internal resistance is lower than PMOS transistors because the electron mobility is higher in NMOS compared to PMOS transistors. Transistor width size increase up to 1100µm and 1500µm for both the transistors (PMOS and NMOS) reduce the internal resistance by 30% and 50% from 750µm width size. The load resistance set is on 2KΩ. It also show that, PMOS have large reduction than NMOS transistor. The proposed circuit using 1500µm PMOS and 750µm NMOS width size give the lower value of internal resistance is 4.60Ω.

(2)In December 2013, IEEE published by Mohad AzrilAb Roap, focuses on the internal resistance of the MOSFET and output power in the CMOS rectifier. In this section, there are two types of analysis on the internal resistance and the analysis to measure the output power of the CMOS rectifier.
The load is set to be 2KΩ and input voltage is 1V. The transistors width size is varied from 10µm to 1200µm. Transistor larger width size obtain bigger current through to the transistor make small value of resistance. The design minimize the problem of lesser mobility in PMOS thus improves drive capability of PMOS. The output power is constant at 4.898x10-4 W for designs 1000µ/750µ to 1500µ/750µ and also has lowest total resistance is 4.60Ω.

(3) In 2012, IEEE presents the study on the CMOS rectifier with low frequency produced by a power plant supply voltage. The paper focuses on the effect of the two different width sizes (4um and 50um). The result for 4um is 558.36mV and increased by 40.6% for 50um width. The MOSFET length is set to constant at 180nm to determine width effect. Thus, the output waveform was analyzed. The simulation was completed with 1V peak voltage and input sine wave is 50Hz using CADENCE simulation software tool. The width size 50µm obtains better output voltage which is 940.46mV than the width size 4µm which has 558.36mV. Therefore, 50µm is 40.6% higher compared the 4µm width. This is the width size of transistor affected the current flow through the MOSFET and overcome the resistance, thus makes the forward voltage decreased.

(4) In this 2009 IEEE, paper titled "High- efficiency differential-drive CMOS rectifier for UHF RFIDs" published by Koji koyani, member IEEE, Atsushi sasaki, and Takashi ito, Senior member IEEE, developed the rectifier can automatically minimize the effective Vth of diode connected MOS transistors in a forward bias condition and automatically increase it in a reverse bias condition by a cross coupled differential circuit configuration. Dependence of the PCE on the input RF signal frequency, output loading conditions and transistor sizing was also evaluated. A test chip was designed and fabricated with a 0.18µm CMOS process having RF option .In NMOS and PMOS transistors width-to-length ratio were 3.6µm/0.18µm and 18µm/0.18µm, respectively and measure Vths were 0.437V and -0.450V respectively. Both coupling capacitor Cc and Cs were designed to be 1.13pF. The output DC voltage reaches its steady state at 15ns from the stating in the case. This paper presents the power conversion efficiency dependence on transistor width size, where NMOS and PMOS transistors are designed to be 3.6µm and 18µm, respectively, a narrower version, where they are 1.8µm and 9µm, a wider version, where they are 7.2µm and 36µm, were designed and measured. The both transistor gate length was fixed at 0.18µm. A CMOS rectifier circuit has large PCE as 67.5% at 953MHz, -12.5 dBm of RF input and load 10KΩ, Thus effective to achieve large output DC voltage without degrading PCE.

(5) In 2007, IEEE published by C. Peters, O. Kessling focused CMOS rectifier are improved the novel architecture for a highly efficient circuit. The rectifier can be fully integrated using a standard CMOS process. A full wave rectifier with only one threshold voltage drop and efficiency 50% is realized and rises up to 90%. In this phenomenon, the maximum power depends on the frequency. The W/l ratio is 700/1 of the transistor depends on the current flow. Smaller transistor widths increase the resistance. In this implementation 3.3V transistors are used with current flowing in only one direction and nearly no voltage drop in output. This circuit has also been simulated using 5V. The overall current consumption is about 3.3µA for an input voltage of 2.75V. The operation range is between 1.6V and 3V.

3. CONCLUSION

The proposed method based on the simulation results. The variation in the width size of the transistors will affect the internal resistance and output voltage drop on the performance of the CMOS rectifier. The smaller width size of the transistor resulted in the large voltage drop in CMOS rectifier. An increase in the width size of the transistor is reducing the voltage drop. Future effort will be focused on the best circuit design since it has low internal resistance and optimum output performance in CMOS rectifier.

REFERENCES

[1] M.A. Ab Raop, R. Radzaun, M.K. Humzah,.;Rahimi M.K.M.S.,"CADENCE Simulation on the Effect of Transistor Width Size on Internal Resistance in CMOS rectifier Using Two PMOS and NMOS" in IEEE , 2013 (ISIEA 2013) , pp. 144-147.

[2] M.A. Ab Raop, R. Radzaun, M.K., Humzah,.;Rahimi.M. K. M. S., "Investigation of different width size of transistor on internal resistance and output power in CMOS rectifier using two PMOS and NMOS" in IEEE, 2013 (SCOReD), pp. 417-420.

[3] Ab Roap M. A.; Radzaun R.; Humzah,M. K.; Rahimi M.M. S.," Effect of different widths in CMOS rectifier for low voltage and frequency application" in IEEE, 2012 (ISCAIE 2012), pp.26-28.

[4] K. Kotani and T. Ito, "High efficiency CMOS rectifier circuits for UHF RFIDs using Vth cancellation techniques," in ASIC, 2009. ASICON '09. IEEE 8th International Conference on, 2009, pp. 549-552.

[5] Peters C.; Kessling O.; Henrici F.; Ortmanns M.; Manoli "CMOS integrated highly efficient full wave rectifier" in IEEE, 2007, pp. 2415-2018.

[6] R. Yuan and D. P. Arnold, "Input-powered energy harvesting interface circuits with zero standby power," in Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE, 2011, pp. 1992-1999.

[7] A. S. W. Man, E. S. Zhang, H. T. Chan, V. K. N. Lau, C. Tsui, and H.C. Luong, "Design and Implementation of a Low-power Baseband system for RFID Tag," in Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on, 2007, pp. 1585-1588

[8] Y. Yuan, S. Yin, and F. F. Dai, "A novel low-power input-independent MOS AC/DC charge pump," in Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on, 2005, pp. 380-383 Vol. 1.

[9] Qiang Li, J.Wang and Y.Inoue, " A two stage CMOS integrated highly efficient rectifier for vibration energy harvesting application" 2014, JICEE Vol. 4 pp336-340.

[10] F.Jiang, D. Guo, L. L. Cheng. "Analysis and design of power generator on passive RFID transponders" Progress in Electromagnetics Research Symposiwm, Hangzhou, China, March 2008.