International Journal of Technology Research and Management
ISSN (Online): 2348-9006
Vol 4 Issue 5 May 2017

A Comparitively Analisis of Various CMOS FINFET Structure

Shraddha Sonone[1], Asst. Prof. Shiva Bhatnagar[2]
M. Tech Student (VLSI Design), Dept. of ECE, Patel College, Indore (M.P.) [1]
Asst. Professor, Dept. of ECE, Patel College, Indore (M.P.) [2]
shraddha.sonone.ec@gmail.com[1], shiva.bhatnagar@patelcollege.com[2]

Abstract: *Fin-type field-effect transistors (FinFETs) are promising substitutes for bulk CMOS at the nano scale. Fin FETs are double-gate devices. The two gates of a FinFET can either be shorted for higher performance or independently controlled for lower leakage or reduced transistor count. This gives rise to a rich design space. This chapter provides an introduction to various interesting Fin FET logic design styles, novel circuit designs, and layout considerations.*

Keywords: *Circuit design, Fin FETs, Layout, Leakage power, Power optimization.*

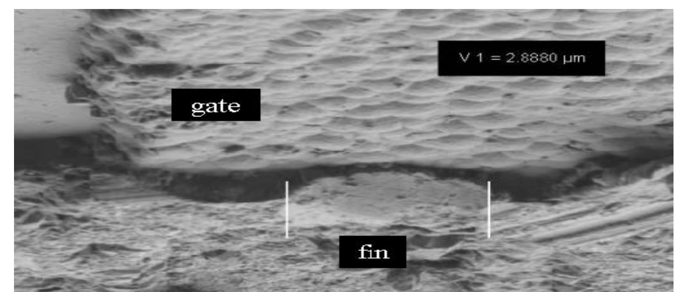
1. INTRODUCTION

As nanometer process technologies have advanced, chip density and operating frequency have increased, making power consumption in battery-operated portable devices a major concern. Even for no portable devices, power consumption is important because of the increased packaging and cooling costs as well as potential reliability problems. Thus, the main design goal for VLSI (very-large-scale integration)designers is to meet performance requirements within a power budget. Therefore, power efficiency has assumed increased importance. This chapter explores how circuits based on Fin FETs (fin-type field-effect transistors), an emerging transistor technology that is likely to supplement or supplant bulk CMOS (complementary metal-oxide-semiconductor) at 22-nm and beyond, offer interesting delay–power tradeoffs'.

The origin of metal-oxide-semiconductor (MOS) device was year 1959. Silicon metal oxide semiconductor field effect transistor (MOSFET) is most important devices in the semiconductor technology (Fig 1.1 NMOS device). The MOSFET used in monolithic integrated circuits (ICs) instead of bipolar junction transistors to perform basic switching operation of digital logic and used as amplifying device in analog as well as digital applications due to it's various advantages. The size of the MOSFET shrunk on very large scale over the years. Scaling was predicted by 'Moore's Law'. Figure 1.2 shows that how number of transistor for different semiconductor industry increase according to Moore's law.[1].

2. QUANTUM EFFECTS

Quantum effect occurs in devices which include tunneling effect. When charge carrier tunnel across barriers of FET, which leads to leakage current. If scaling continues, it will leads to higher power dissipation. Higher electrostatic field 105 V/cm across reverse bias PN junction causes major current to flow through junction because of tunneling of electrons from valence band of p region to conduction band of n region, for tunneling to arise, total voltage drop across the junction need to be higher than band gap. So modeling at very small dimension is very crucial task. [1].



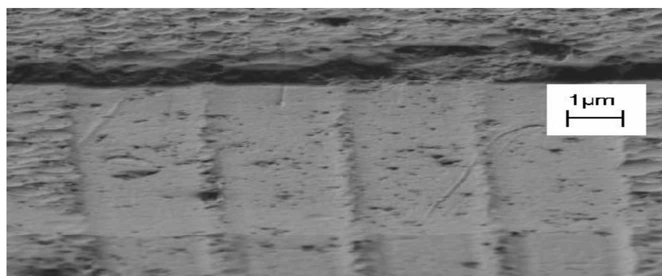


Fig (1) Region of DOUBLE GATE

3. FINFET BENEFITS, DRAWBACKS AND ALTERNATIVES

The multiple research efforts in the FinFET arena have already produced impressive results from both academia and industry. However, FinFETs are not the only solution to the problems of continued scaling. The first and most obvious approach is to continue with traditional planar CMOS technologies until a fundamental barrier, such as the size of the silicon atom, is achieved. The costs associated with transition to entirely new types of devices are immensely prohibitive, considering the time and investment needed to establish new design and manufacturing processes. Thus, the transition to new and riskier solutions is a tremendous undertaking, with the industry focusing on an approach that works and works now. Still, short-sightedness is a quality that is not highly regarded, and most major manufacturers and researchers have investigated alternatives to both planar CMOS and FinFETs. the size of the silicon atom, is achieved. The costs associated with transition to entirely new types of devices are immensely prohibitive, considering the time and investment needed to establish new design and manufacturing processes. Thus, the transition to new and riskier solutions is a tremendous undertaking, with the industry focusing on an approach that works and works now. Still, short-sightedness is a quality that is not highly regarded, and most major manufacturers and researchers have investigated alternatives to both planar CMOS and FinFETs. The “multi-gate” FET device group, to which FinFETs belong, contains several proposed solutions to scaling problems. For example, researchers have already demonstrated functioning double-gate (DG) planar devices [2] and gate-all-around(GAA) devices [2]. These types of FETs offer benefits similar to those of FinFETs: improved short-channel effects and sub threshold slope, with an increased drive current density. However, while the effective transistor width of a FinFET is controlled by the number of fins present, planar DG devices are thought to be limited in width to less thane micron, while GAA devices often present tremendous design and process difficulties in Manufacturing.

For the standard cell test, we set FO4 load, which assumes each standard cell in the system has an average fan-out of four inverters (INVs). The input signal slew is set to be 15ps. The power is measured by testing the average dynamic power of all switching scenarios. The power of each standard cell is measured assuming the same input signal frequency of 1GHz. The delay is measured by taking the worst case propagation delay. Normalized evaluation results.

The 3D INV, NAND2, NOR2, DFF cells show up to 13% delay reduction, around 11% lower power, and 44% reduced footprint compared to the 2D cells. For the redesigned cells NAND3, AOI21 and AOI22, we achieve up to 22% reduced delay, around 20% lower power, and 55% reduced footprint compared to 2D designs. Related to this, Table III shows the effective internal capacitance values in 3D cells vs. 2D cells.

4. COMPARISION BETWEEN SOI AND FINFET TECHNOLOGY

Alternative of MOSFET device structure is based upon silicon-on-insulator (SOI) technology has emerged as an effective measure of extending MOS scaling beyond the limit of bulk for low- power or high-performance applications. Partially depleted SOI was the 1st SOI technology which introduced for high-performance microprocessor. The ultra thin body fully depleted SOI and non-planar Fin FET device structures are promising to be potential future of technology or device choices. [6][7][8]

Partially depleted silicon on insulator (PD SOI) transistor shown in Fig.1.4 is a layer of SiO_2 which separates upper device contains silicon film and rest of the Si substrate. Silicon film is comparatively thick (~90 nm or more). In the off condition, with no voltage applied to gate terminal, the maximum width of depletion region underneath gate oxide is smaller than silicon film thickness. The lower region of partially depleted SOI has a quasi-neutral region which is left noncontact. Potential of floating Si area is calculated by capacitive coupling of different electrodes dynamically and in steady state, by forward and reverse biased currents to drain and source junctions, which leads to various floating body effects like parasitic bipolar kink effect and history dependent threshold voltage. The major advantage of the partially depleted device is somewhat lower leakage and

higher speed due to reduced drain and source region junction capacitances. By using ion implantation, the floating body effects could be reduced or by placing body contact. Although, from electrostatic scalability and static leakage point of view, PD SOI device looks like bulk FET. Therefore, it is not be scaled beyond what can be achieved with well design bulk FET. [4]

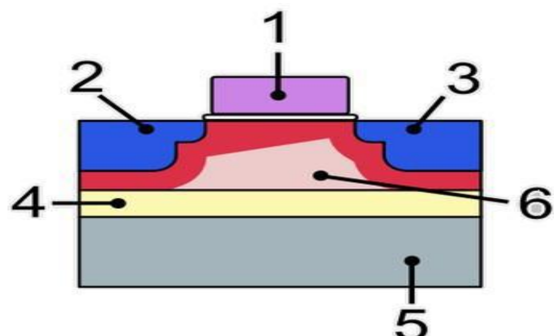


Fig (2) Structure of soi and FINFET

5. OTHER TRADITIONAL APRROCH TO DESIGN OF FINFET

1. LEKAGE CURRENT: The traditional MOS generation is getting major difficulty because of various causes like increased off state current, large power consumption, mobility degraded and various kind of SCE. For reduction of these, severe impacts on device, various SOI devices are suggested and examined like double gate, pi gate, all around gate and omega gate. Amid all such devices, narrow fin based FET gained more popularity because of favorable exoneration to short channel effects, sub threshold swing, higher carrier mobility and higher drain current. [2][6][7][8][9].

Silicon on insulator based Fin FET device has diverse benefits as compare to traditional Fin FET like smaller off state current, smaller source to substrate capacitor and drain to substrate capacitor, large drain current, superior sub threshold characteristics, and less sensitiveness to doped body. Other sides, traditional Fin FET has benefits of smaller price of manufacturing, smaller fault density, lower self heating, and highly stable against “negative bias temperature instability”. In conventional Fin FETs difficulty of “threshold voltage roll off” could eradicate using increased under-lap length. [2][6][7][8][1]

2. EFFECT OF POWER DISSIPATION: 2003[2] explained that why large leakage current in scaled down device become major cause to power consumption in MOS transistor while channel length, gate oxide thickness and threshold voltage reduced. Resulting, to find and modeling of various leakage elements are significant to reckon and decrease of leakage power, particularly for small power application. This paper analysis different device leakage process, comprising weak inversion, DIBL, GIDL, and tunneling through oxide. Channel engineering method comprising retrograde well and halo doping is examined to reduce SCE for constant scaling of MOS transistor. Lastly, paper analyzed various circuit methods to minimize leakage power dissipation.

3. PSP TECHNOLOGY: 2007[4] examined progression on partially depleted (PD) SOI modeling utilizing surface potential base method. Newly design model said “PSP SOI” model, which constructed within current industrial standard of conventional MOS device PSP model. Besides physics based approach and scalability inheritance from PSP, PSP SOI apprehend SOI precise effects using inclusion of floating body simulation capacity, parasitic bipolar model, and self-heating. The PSP SOI model verified over various PD/SOI technology.

4. COUPLING OF ELECTRIC FINFET: 2012 [1] investigated how ground plane decrease coupling of electric field between source and drain to decrease DIBL. Ground plane (GP) method is one of the methods used to decrease the DIBL effect in SC SOI device. This method suitable if distance between GP and drain is negligible liken to channel length. GP transistor showed smaller leakage power dissipation liken to transistor with no GP. GP FinFET device, as GP remove DIBL effect, it’s reliance over channel doping density is reckon weakened. Hence, to reduce random doping variation, such device used with smaller channel doping density with no concerned of DIBL.

5. THRESHOLD VARIATION: in 2013 [3] analyzed how can SCE be reduce in Fin FET. Simulation shows that Fin FETs device can be scale to 8 nm. Very thin fin enables to reduce SCE. The SCE is limited by physical structure and off state leakage is decrease using ultra fine Si film in Fin FETs structure. For better reduction of leakage current, the thickness of Si film must be lesser then one fourth the channel length. Threshold voltage can be change by changing work function using mid gap material.

6. SPEED AND SYNCHRONIZATION: 2013 [6] showed that SOI Fin FETs of Thin Fin width compare to SGOI(Silicon Germanium on Insulator) MOSFET Body thickness, provide great control to SCE and decreased power consumption because of decreased gate leakage current. Using different spacer width and Fin width, transistor performance improved. The performance of triple gate FinFETs compare to Ultra Thin Body (UTB) Recessed Source drain SGOI MOSFET in forms of delay, power dissipation and noise margin for a CMOS inverter and results indicate the better suitability of SOI FinFET structures for Low standby Power (LSTP) Application. SOI FinFET device Sensitivity to process parameters such as Gate Length, Spacer Width, Oxide thickness, Fin Width, Fin Height and Fin doping have examined and reported.

7. SWITCHING FUCTION IN FINFT: 2015 [1] analyzed simulative data achieve using TCAD tool for 3D SOI FinFET device for gate length of 8 nm at room temperature. The impact of changing device main electrical parameter, like threshold voltage, sub threshold slope, trans conductance, DIBL, on current, leakage current and on/off current ratio are presented and analyzed, also explain impact of gate work function variation on device. This changes direct influence on electrical characteristic. Results describe that threshold voltage reduce as reduce the gate metal work function. Consequently, leakage current improves with increase work function.

6. OBJECTIVES OF PREVIOUS RESEARCH

1. To reduce the short channel effects by varying the under lap length and doping,
2. To reduce leakage current and DIBL effects by varying fin height and width,
3. To reduce sub threshold leakage current by varying oxide thickness for double and triple gate Fin FET.

7. SERVEY OF DOUBLE GATE AND TRIPPEL GATE FINFET

DOUBLE GAT FINFET: Double gate MOSFET is becoming an intense subject of VLSI research because in theory, it can be scaled to the shortest channel length possible for a given gate oxide thickness. But the difficulty in fabrication of DG MOSFET) is encountered due to the misalignment of top gate and the back gate. Hence to eliminate the misalignment of gates in DG MOSFET, FinFET considered one of the most promising candidates for future generation transistor technologies due to their excellent electrostatic integrity such as Low leakage current, improved short channel effect, high performance resulting from the undoped channel structure, high carrier mobility and reduction of random dopant fluctuation. With the scaling of the devices, the fins needed to be thinner due to which scattering of dopants increases. Hence, lightly doped fins are preferred to reduce the scattering or random dopant fluctuations. [6]

TRIPLE GATE FINFET : Modern FinFETs are 3D structures that rise above the planar substrate, giving them more volume than a planar gate for the same planar area. Given the excellent control of the conducting channel by the gate, which “wraps” around the channel, very little current is allowed to leak through the body when the device is in the off state. This allows the use of lower threshold voltages, which results in optimal switching speeds and power. [6]The different ways in which the gate electrode can be wrapped around the channel region of a transistor are shown in the Figure 3.All the structure has its own advantages.

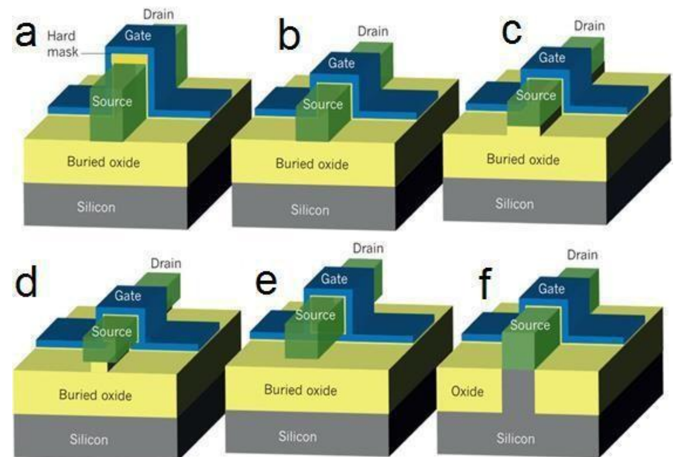


Fig (3) 3D STRUCTURE OF SOI AND FIN FET

8. CONCULUSION AND FUTURE SCOPE

From the results, it is concluded that Fin FETs are extremely fast and power efficient devices, as device dimension is scaled down to smaller technology, its drive current is very large in comparison to leakage current that means ratio of on to off current is very large. The multi-gate structures lead to great supremacy over inversion layer and give small SCEs. The Fin FETs are difficult to fabricate with excellence due to its smaller size (nano scale). Changes in physical structures, dimensions and different material are

utilized to achieve higher drive current, speed, and threshold voltage. Off state current increased with increased fin width due to lack of gate control over the channel area, so we need to keep fin width under control to improves DIBL. The off state current decrease with decrease in fin-width as center part of fin getting more grips from gate.

With decrease in fin height, off state current reduces due to increasing of parasitic resistances. The Extended fin height offers more resistance in comparison of smaller fin height, which leads to low off state current. Gate capacitances due to fringing electric field reduces due to increase in underlap length and hence a decrease in off state current. Also as under lap length increases the sub-threshold slope improves and drain induced barrier lowering reduces.

To further scaled down the dimension of FinFET various short channel and nano channel effects comes in the picture. To overcome this effects the MOSFET structure are need to modified as well as channel engineering and new materials are required.

REFERENCES

[1] Y. Tsividis, Operation and Modeling of The MOS Transistor, Lattice Press, 2000, p. 277-279.
[2] Y. Tsividis, Operation and Modeling of The MOS Transistor, Lattice Press, 2000, p. 258.
[3] B. Mann, “Development of Thin Gate Oxides for Advanced CMOS Applications,” RIT 22nd Annual Microelectronics Engineering Conference, May 2004.
[4] Y. Tsividis, Operation and Modeling of The MOS Transistor, Lattice Press, 2000, p. 54.
[5] S. Wolf and R. N. Tauber, Silicon Processing for the VLSI Era, Vol. 1: Process Technology, WCV McGraw-Hill, 1999, p. 289.
[6] S. Wolf and R. N. Tauber, Silicon Processing for the VLSI Era, Vol. 1: Process Technology, WCV McGraw-Hill, 1999, p. 293.
[7] F. Montillo and P. Balk, "High-temperature Annealing of Oxidized Silicon Surfaces," J. Electrochem. Soc., vol. 118, pp. 1463-1468, 1971.
[8] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, “On the Universality of Inversion Layer Mobility inSi MOSFET’s: Part II – Effects of Surface Orientation,” IEEE Trans. Elec. Dev., vol. 41, no. 12, pp. 2363-2368, 1994.
[9] B. Yu, L. Chang, S. Ahmed, Haihong Wang, S. Bell, Chih-Yuh Yang, C. Tabery, Chau Ho, Qi Xiang,Tsu-Jae King, J. Bokor, Chenming Hu, Ming-Ren Lin, and D. Kyser, “FinFET scaling to 10 nm gatelength,” in IEDM Tech. Dig., 2002, pp. 251-254.
[10] Y.-K. Choi, L. Chang, P. Ranade, J.-S. Lee, D. Ha, S. Balasubramanian, A. Agarwal, M. Ameen, T.-J.King, and J. Bokor, “FinFET Process Refinements for Improved Mobility and Gate Work Function Engineering,” in IEDM Tech. Dig., 2002, pp. 259-262.
[11] B. Goebel, D. Schumann, and E. Bertagnolli, “Vertical N-Channel MOSFETs for Extremely High Density Memories: The Impact of Interface Orientation on Device Performance,” IEEE Trans. Elec. Dev.,vol. 48, no. 5, pp. 897-906, 2001.